

**301402****May, 2019****B.Tech. - IV SEMESTER****Computer Organization & Architecture (PCC-CS-402)**

Time : 3 Hours]

[Max. Marks : 75

**Instructions :**

1. It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.
2. Answer any four questions from Part-B in detail.
3. Different sub-parts of a question are to be attempted adjacent to each other.



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**PART-A**

1. (a) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two address instructions, how many one-address instructions can be formulated? (1.5)
- (b) Execute and share the result when Logical X-OR operation is applied to  $(4ACO)_{16}$  &  $(B53F)_{16}$ . (1.5)
- (c) Differentiate between decoder and demultiplexer. (1.5)
- (d) Why are addressing modes necessary in computer architecture? (1.5)
- (e) Represent  $(-18)$  in signed 1's complement and signed 2's complement representation. (1.5)



Dislike



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Share

- (f) An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in the address and memory spaces? (1.5)
- (g) Represent the following conditional statement by two register transfer statement with control functions.  
If  $(P=1)$  then  $(R1 \rightarrow R2)$  else if  $(Q=1)$  then  $(R1 \leftarrow R3)$ . (1.5)
- (h) What does CMA, ISZ, SNA, SKI, ION signifies? (1.5)
- (i) Explain the terms : seek time, rotational latency, and transfer time. (1.5)
- (j) A bus has 16 data lines and requires 4 cycles of 250 ns each to transfer data. The bandwidth of the bus is 2 MBps. If the cycle time of the bus is reduced to 125 ns what would be the bandwidth of the bus? (1.5)

### PART-B

2. (a) Design 4-bit by 4-bit array multiplier. Use AND gate and Binary adder. (4)
- (b) Give a flowchart for add and subtract operations. (2)
- (c) Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers for holding signed numbers. Multiplicand is +5:
- (i)  $(+5) \times (+3)$
- (ii)  $(+5) \times (-3)$ . (4)

- (d) Show the contents of registers E, A, Q and SC during the process of division of
- (i) 10100011 by 1011
  - (ii) 11110000 by 0011.
- (use a dividend of 8bits). (4)

3. (a) Draw the timing diagram assuming that  $SC = 0$  at the time  $T3$  if control signal  $C7$  is active  $C7T3 : SC \rightarrow 0$ .  $C7$  is activated with the positive clock transition associated with  $T1$ . (5)
- (b) Discuss the different addressing modes. Also highlight the difference between indexed addressing and base register addressing modes? (6)
- (c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative, and (iv) indirect. (4)

4. (a) Explain the three types of mapping procedures used in the organization of cache memory. (10)
- (b) A computer uses RAM chips of  $1024 \times 1$  capacity
- (i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes.
  - (ii) How many chips are needed to provide a memory capacity of 16K Bytes ?
- Show the connection diagram for the same. (3)

(c) What is miss rate and miss penalty? (2)

5. (a) Give a brief architecture of 8086 microprocessor. (5)
- (b) Discuss the different types of instructions that are commonly incorporated in computer systems. Also explain three instructions of each type for Berkeley RISC I. (7)
- (c) Differentiate between RISC and CISC instruction sets. (3)

6. (a) What is asynchronous data transfer? Discuss asynchronous data transfer using (i) strobe control and (ii) handshaking with timing and block diagram. (8)
- (b) Discuss different modes of DMA data transfer. (7)

7. (a) Differentiate between programmed I/O and interrupt-driven I/O. What is basic advantage of using interrupt-initiated data transfer over transfer under program control without interrupt? (7)

(b) Give Flynn's Classifications of parallel processors.

(c) What do you mean by memory and cache coherence? (4)



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